

20V P-Ch Power MOSFET

Feature

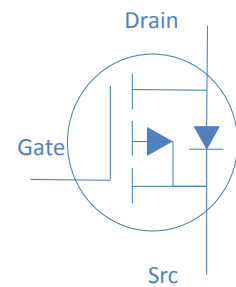
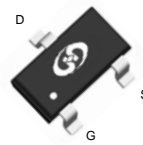
- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Avalanche Ruggedness
- ◇ Lead Free, Halogen Free

Application

- ◇ Load Switches
- ◇ Hard Switching and High Speed Circuit
- ◇ BLDC Motor

V_{DS}		-20	V
$R_{DS(on),typ}$	$V_{GS}=4.5V$	53	mΩ
$R_{DS(on),typ}$	$V_{GS}=2.5V$	75	mΩ
$R_{DS(on),typ}$	$V_{GS}=1.8V$	150	mΩ
I_D (Silicon Limited)		-4	A

SOT-23



Part Number	Package	Marking
HTJ650P02	SOT-23	25

Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	$T_A=25^\circ\text{C}$	-4	A
		$T_A=70^\circ\text{C}$	-2.8	
Drain to Source Voltage	V_{DS}	-	-20	V
Gate to Source Voltage	V_{GS}	-	± 12	V
Pulsed Drain Current	I_{DM}	-	-16	A
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	1.04	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	$^\circ\text{C}$

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	120	$^\circ\text{C/W}$

Electrical Characteristics at $T_j=25^\circ\text{C}$ (unless otherwise specified)
Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-0.3	-0.75	-1.2	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=-16V, T_j=25^\circ\text{C}$	-	-	-1	μA
		$V_{GS}=0V, V_{DS}=-16V, T_j=125^\circ\text{C}$	-	-	-10	
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-3.5A$	-	53	65	m Ω
		$V_{GS}=-2.5V, I_D=-2.5A$	-	75	96	
		$V_{GS}=-1.8V, I_D=-1A$	-	150	250	
Transconductance	g_{fs}	$V_{DS}=-5V, I_D=-3.5A$	-	10	-	S

Dynamic Characteristics

Input Capacitance	C_{iss}		-	382	-	pF
Output Capacitance	C_{oss}	$V_{GS}=0V, V_{DS}=-10V, f=1\text{MHz}$	-	70	-	
Reverse Transfer Capacitance	C_{rss}		-	60	-	
Total Gate Charge	Q_g		-	7.2	-	nC
Gate to Source Charge	Q_{gs}	$V_{DD}=-10V, I_D=-3.5A, V_{GS}=-4.5V$	-	1.2	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	2.3	-	
Turn on Delay Time	$t_{d(on)}$		-	17	-	ns
Rise time	t_r	$V_{DD}=-10V, I_D=-1A, V_{GS}=-4.5V,$	-	32	-	
Turn off Delay Time	$t_{d(off)}$	$R_G=6\Omega,$	-	37	-	
Fall Time	t_f		-	32	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_F=-3A$	-		-1.2	V
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Fig 1. Typical Output Characteristics

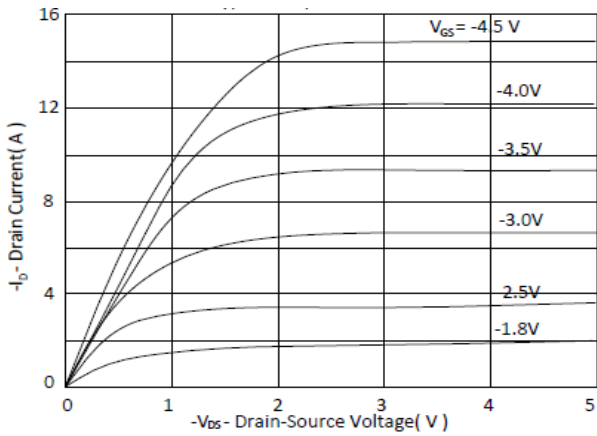


Figure 2. On-Resistance vs. Gate-Source Voltage

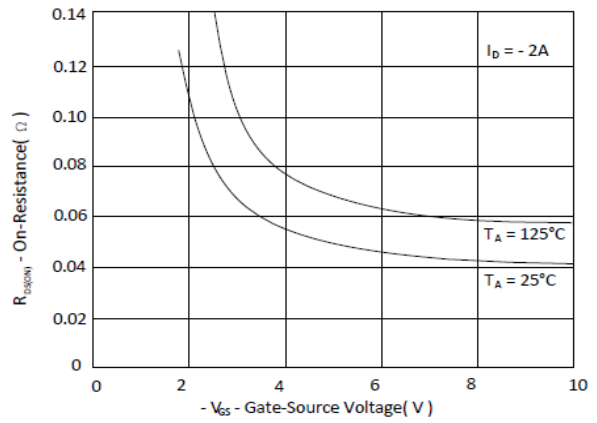


Figure 3. Gate Threshold Voltage v.s. Junction Temperature

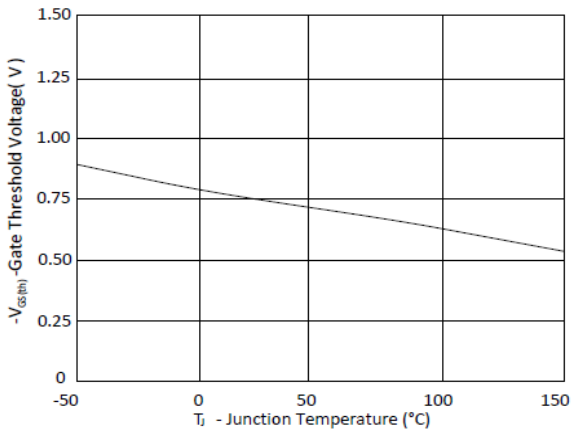


Figure 4. Normalized On-Resistance vs. Junction Temperature

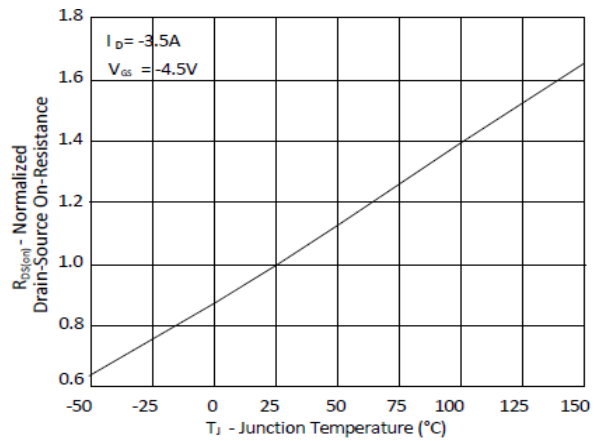


Figure 5. Typical Source-Drain Diode Forward Voltage

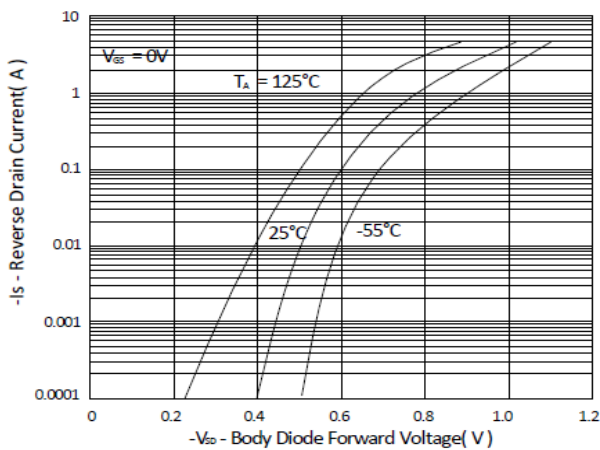


Figure 6. Typical Gate-Charge vs. Gate-to-Source Voltage

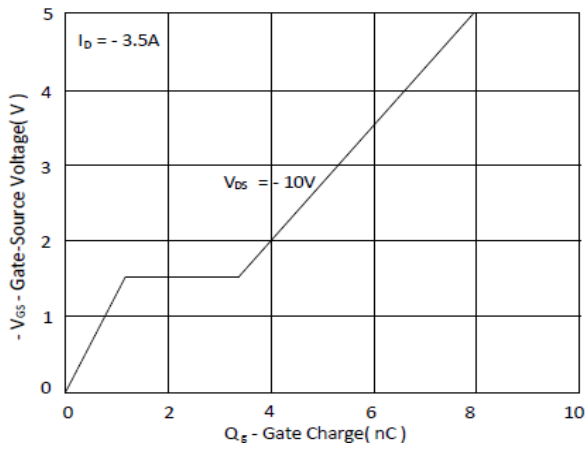


Figure 7. Typical Capacitance vs. Drain-to-Source Voltage

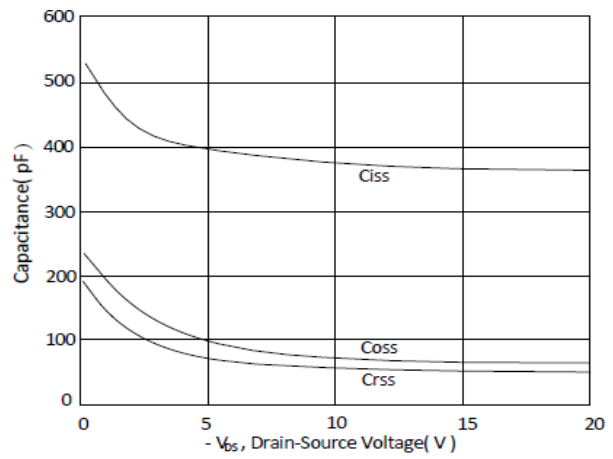


Figure 8. Maximum Safe Operating Area

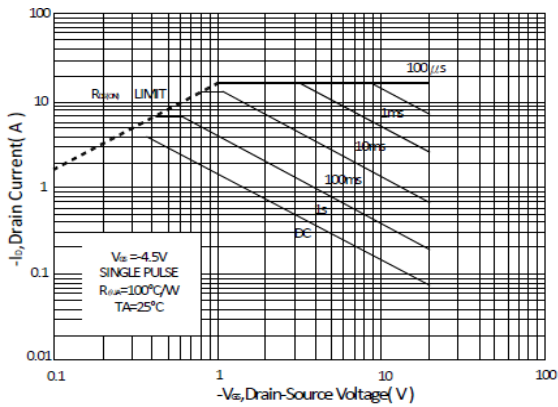


Figure 9. Single Pulse Maximum Power Dissipation

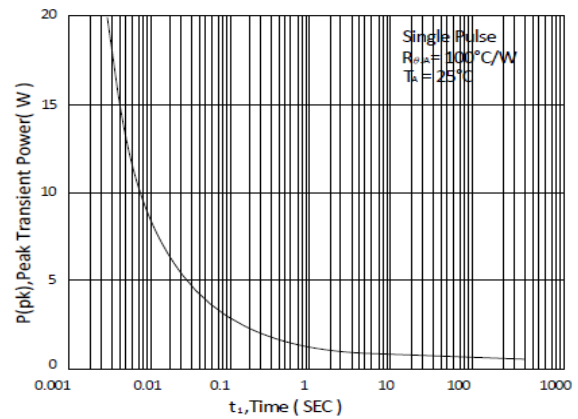
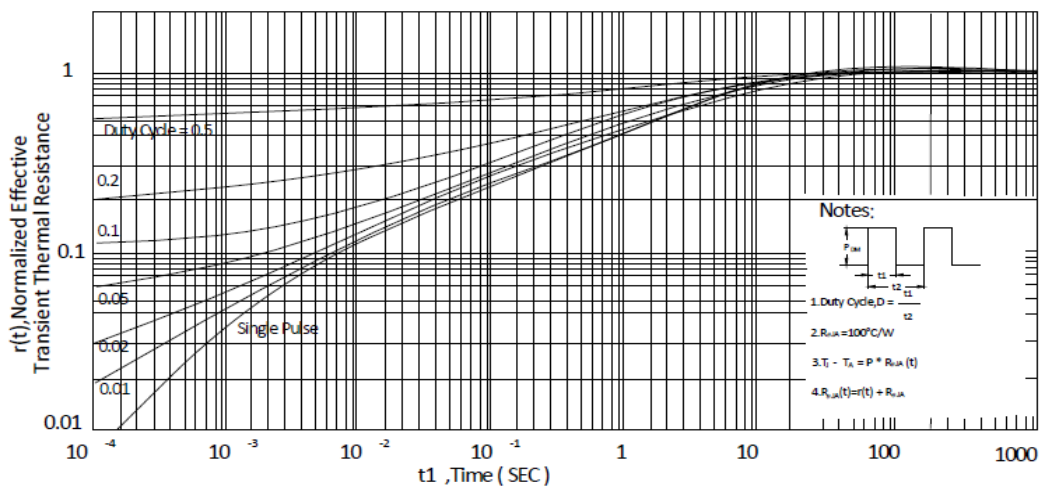
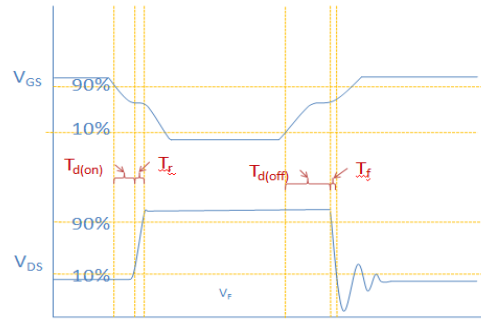
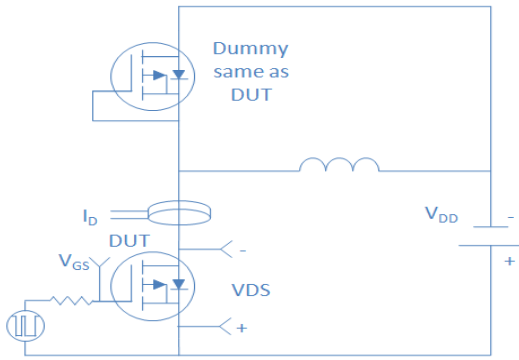


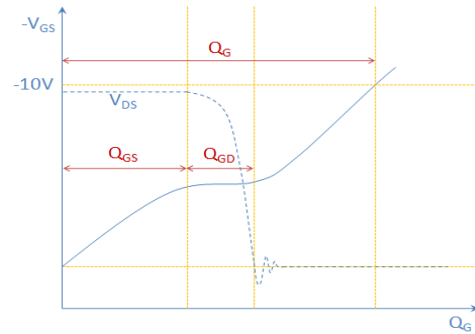
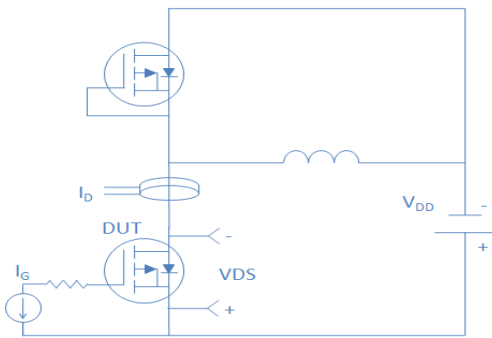
Figure 10. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



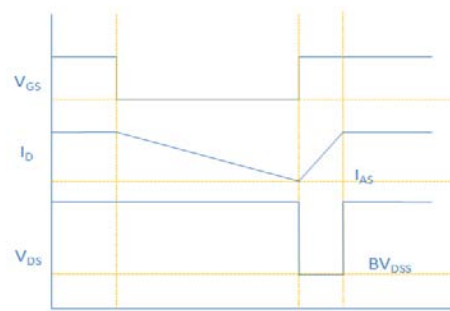
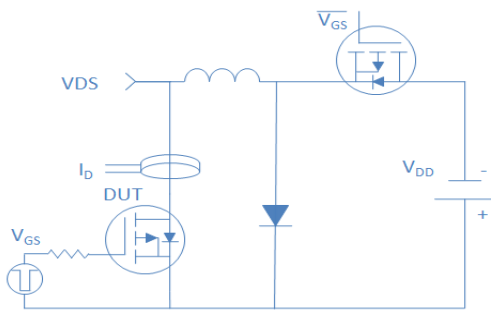
Inductive switching Test



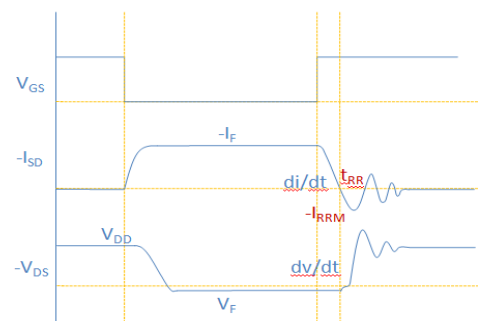
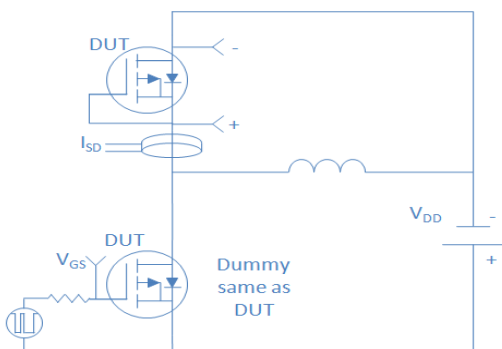
Gate Charge Test



Uclamped Inductive Switching (UIS) Test

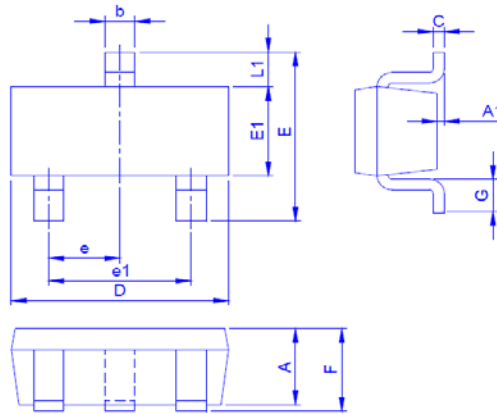


Diode Recovery Test



Package Outline

SOT-23, 3leads



Dimension in mm

Dimension	A	A1	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.70	0	0.3	0.08	2.80	2.25	1.2	0.90		0.80	0.3	0.50
Typ.					2.90			0.95	1.9			
Max.	1.15	0.1	0.5	0.20	3.02	3.00	1.7	1.00		1.25	0.6	0.75